RECORD OF TELEPHONE INTERVIEW

Undersigned Attorney for Applicant thanks Examiner Takaoka for the courtesy extended during the telephone interview conducted on January 25, 2005. The parties discussed Claims 1 and 11 and a number of references including Nishikawa, U.S. Pat. No. 5,634,208 and Koch, 5,032,803. Several potential claims to overcome the references were discussed, but no agreement was reached with respect to any particular claims other than the claims indicated as allowable in the Official Action.

STATUS OF CLAIMS

Applicant also thanks Examiner Takaoka for his careful examination of the present application. Claims 1-10, 14-17, 21-29 and 31-37 stand rejected. Claims 11-13, 18-20 and 30 are objected to but indicated as allowable. In the concurrently filed Amendment, Applicant has amended the original claims the extent believed necessary to place the claims in condition for allowance. These amendments are described in detail below along with Applicants statement of the reasons why the amended claims are allowable.

REMARKS

Applicant submits that the most relevant references are Nishikawa, U.S. Pat. No. 5,634,208, Koch, U.S. Pat. No. 5,032,803 and Veitschegger, U.S. Pat. No. 5,486,798. Nishikawa shows a number of different double-sided microstrip signal processing networks implemented on printed circuit boards. Although some circuits have multiple ports located on the same interface edge, none of the circuits have input and output ports located on the same interface edge. See, Fig. 12 and col. 11, lines 1-10 (port 71 is an input port and ports 72, 73 and 74 are output ports); Fig. 15 and col. 11, lines 30-34 (port 71 is an input port and ports 72 and 74 are output ports, port 73 is inert); Figs. 16-18 and col. 11, lines 35-50 (same I/O configuration as Fig. 15); Figs. 26-28 (ports 71 and 73 are inputs, 72 and 74 are outputs); Figs. 33-35 (ports 71 and 73 are inputs, 72 and 74 are outputs); Figs. 36-38 (ports 71 and 73 are inputs, 72 and 74 are outputs).

In addition, none of the Nishikawa circuits implement a Butler matrix or a circuit selected from the group consisting of a two-by-four beam steering circuit; a diplexer filter circuit comprising at least three ports; a four-by-four Butler matrix circuit; an eight-

by-eight Butler matrix circuit; and monopulse comparator circuit. See col. 6, line 10 – col. 7, line17. And all of the Nishikawa circuits have an air-exposed microstrip on one side and a dielectric-exposed microstrip on the opposing side. See Figs. 1A, 1B, 3A, 3B, 4A, 4B, 21, 22, 37, and 41. That is, none of the Nishikawa circuits have an air-exposed microstrip on both sides, dielectric-exposed microstrip on both sides, or ground planes on both sides.

Koch shows an edge-mounted crossover card, which does include two input ports and two output ports at the same interface edge. But Koch does not disclose a circuit implementing a Butler matrix or a circuit selected from the group consisting of a two-by-four beam steering circuit; a diplexer filter circuit comprising at least three ports; a four-by-four Butler matrix circuit; an eight-by-eight Butler matrix circuit; and a monopulse comparator circuit. In addition, the Koch circuit board does not include an internal ground plane. Instead, outer layer 24 is a copper ground plane. See Figs. 3-4 and col. 3, lines 41-48. Like Nishikawa , none of the Koch circuits have an air-exposed microstrip on both sides, dielectric-exposed microstrip on both sides, or ground planes on both sides.

Veitschegger shows a double-sided microstrip circuit board with a ground plane and a transmission circuit on both sided of the board. Veitschegger does not disclose an internal ground plane or a circuit implementing a Butler matrix or a circuit selected from the group consisting of a two-by-four beam steering circuit; a diplexer filter circuit comprising at least three ports; a four-by-four Butler matrix circuit; an eight-by-eight Butler matrix circuit; and a monopulse comparator circuit.

Original claims 1-37 have been amended to recite that "the first and second stripline circuits comprise a Butler matrix circuit configured for a carrier frequency" or "a circuit selected from the group consisting of a two-by-four beam steering circuit; a diplexer filter circuit comprising at least three ports; a four-by-four Butler matrix circuit; an eight-by-eight Butler matrix circuit; and a monopulse comparator circuit." None of the references disclose a double-sided circuit with input and output ports located on a common interface edge implementing any of these circuits. Nor is it obvious how to implement any of these circuits on a double-sided circuit board based on the cited references. As a result, the cited references cannot be combined to establish a prima-facie case of obviousness. MPEP § 2143.03.

Therefore, the Applicant respectfully submits that the claims, as amended, are patentable over the cited references and that the present application is in condition for allowance.

CONCLUSION

It is believed that the preceding remarks are completely responsive to the First Official Action mailed November 30, 2004, and that the claims are in condition for allowance. If Examiner Takaoka believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an Examiner's amendment, please call Mike Mehrman at (404) 497-7400.

Respectfully submitted,

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